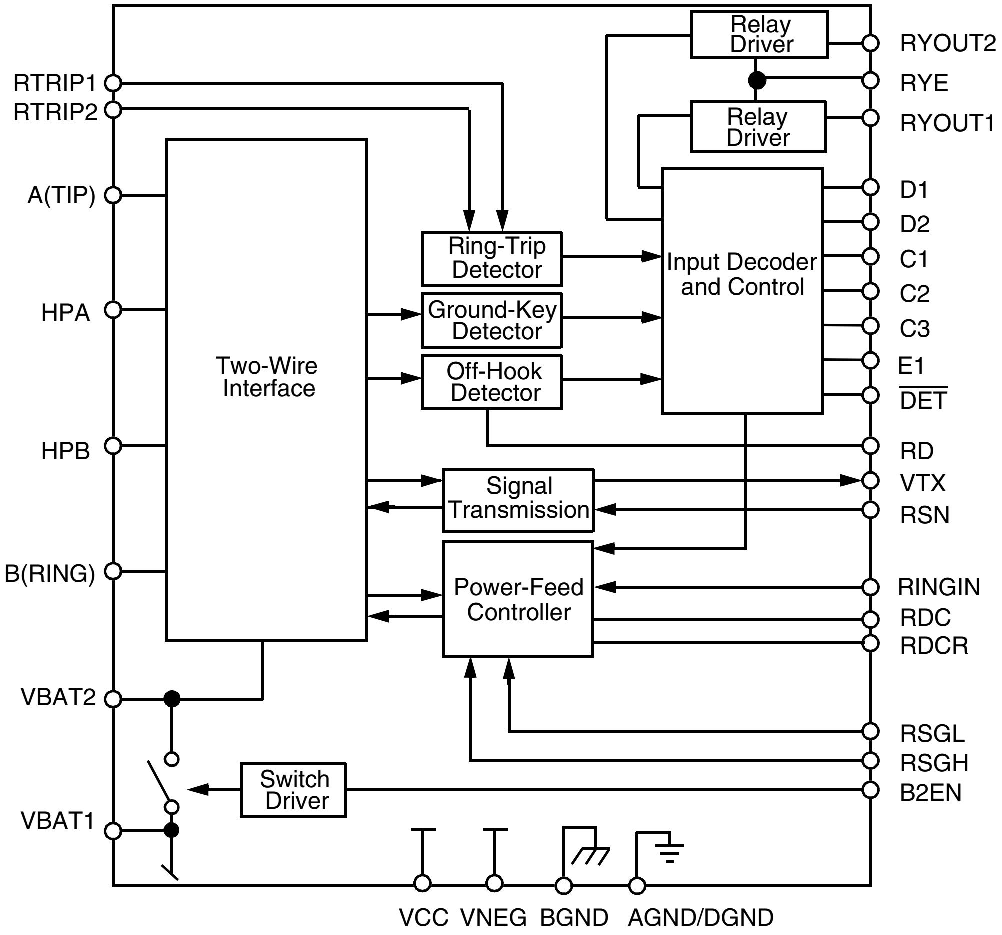
Am79R70

Ringing Subscriber Line Interface Circuit

DISTINCTIVE CHARACTERISTICS

- Ideal for ISDN-TA and set top applications
- On-chip ringing with on-chip ring-trip detector
- Low standby state power
- Battery operation:
  - — V_{BAT1}: –40 V to –67 V
  - — V_{BAT2}: –19 V to V_{BAT1}
- On-chip battery switching and feed selection
- On-hook transmission
- Polarity reversal option
- Programmable constant-current feed
- Programmable Open Circuit voltage
- Programmable loop-detect threshold
- Current gain = 1000
- Two-wire impedance set by single component
- Ground-key detector
- Tip Open state for ground-start lines
- Internal V_{EE} regulator (no external –5 V power supply required)
- Two on-chip relay drivers and snubber circuits

BLOCK DIAGRAM



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GENERAL DESCRIPTION

The AMD family of subscriber line interface circuit (SLIC) products provide the telephone interface functions required throughout the worldwide market. AMD SLIC devices address all major telephony markets including central office (CO), private branch exchange (PBX), digital loop carrier (DLC), fiber-in-the-loop (FITL), radio-in-the-loop (RITL), hybrid fiber coax (HFC), and video telephony applications.

The AMD SLIC devices offer support of BORSHT (battery feed, overvoltage protection, ringing, supervision, hybrid, and test) functions with features including current limiting, on-hook transmission, polarity reversal, tip-open, and loop-current detection. These features allow reduction of linecard cost by minimizing component count, conserving board space, and supporting automated manufacturing.

The AMD SLIC devices provide the two- to four-wire hybrid function, DC loop feed, and two-wire supervision. Two-wire termination is programmed by a scaled impedance network. Transhybrid balance can be achieved with an external balance circuit or simply programmed using a companion AMD codec device, the Am79C02/03/031 DSLAC™ device, the Am79Q02/021/031 Programmable Quad SLAC (QSLAC™) device, or the Am79Q5457/4457 Nonprogrammable QSLAC device.

The Am79R70 Ringing SLIC device is a bipolar monolithic SLIC that offers on-chip ringing. Now designers can achieve significant cost reductions at the system level for short-loop applications by integrating the ringing function on chip. Examples of such applications would be ISDN Terminal Adaptors and set top boxes. Using a CMOS-compatible input waveform and wave shaping R-C network, the Am79R70 Ringing SLIC can provide trapezoidal wave ringing to meet various design requirements.

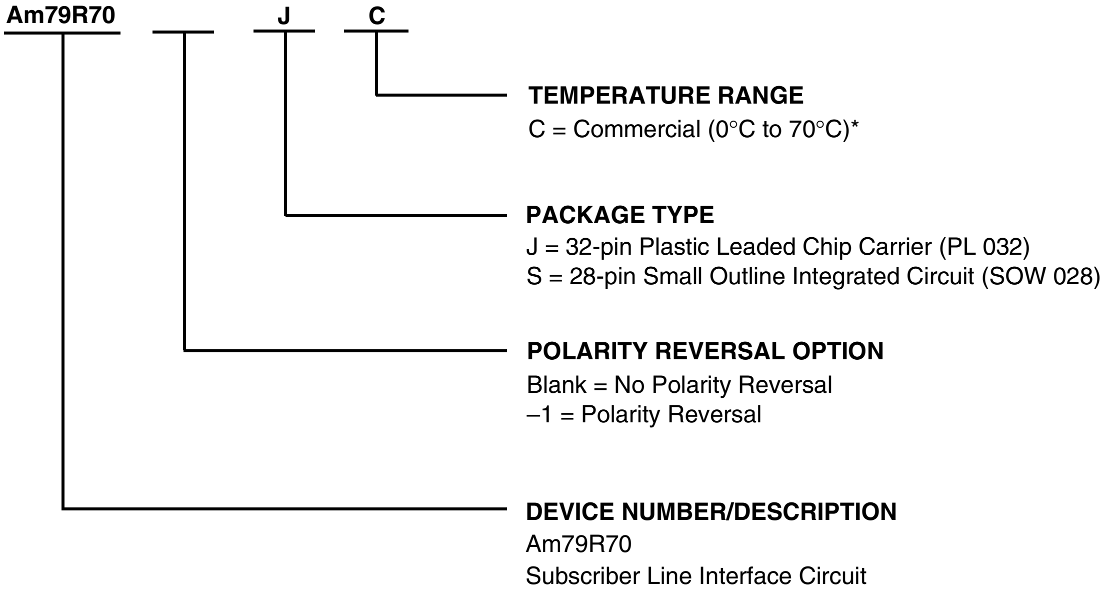
In order to further enhance the suitability of this device in short-loop, distributed switching applications, AMD has maximized power savings by incorporating battery switching on chip. The Am79R70 Ringing SLIC device switches between two battery supplies such that in the Off-hook (active) state, a low battery is used to save power. In order to meet the Open Circuit voltage requirements of fax machines and maintenance termination units (MTU), the SLIC automatically switches to a higher voltage in the On-hook (standby) state.

Like all of the AMD SLIC devices, the Am79R70 Ringing SLIC device supports on-hook transmission, ring-trip detection and programmable loop-detect threshold. The Am79R70 Ringing SLIC device is a programmable constant-current feed device with two on-chip relay drivers to operate external relays. This unique device is available in the proven AMD 75 V bipolar process in 32-pin PLCC packages.

ORDERING INFORMATION

Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of the elements below.



TEMPERATURE RANGE
C = Commercial (0°C to 70°C)*

PACKAGE TYPE
J = 32-pin Plastic Leaded Chip Carrier (PL 032)
S = 28-pin Small Outline Integrated Circuit (SOW 028)

POLARITY REVERSAL OPTION
Blank = No Polarity Reversal
–1 = Polarity Reversal

DEVICE NUMBER/DESCRIPTION
Am79R70
Subscriber Line Interface Circuit

Valid Combinations		
Am79R70	–1	JC SC

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

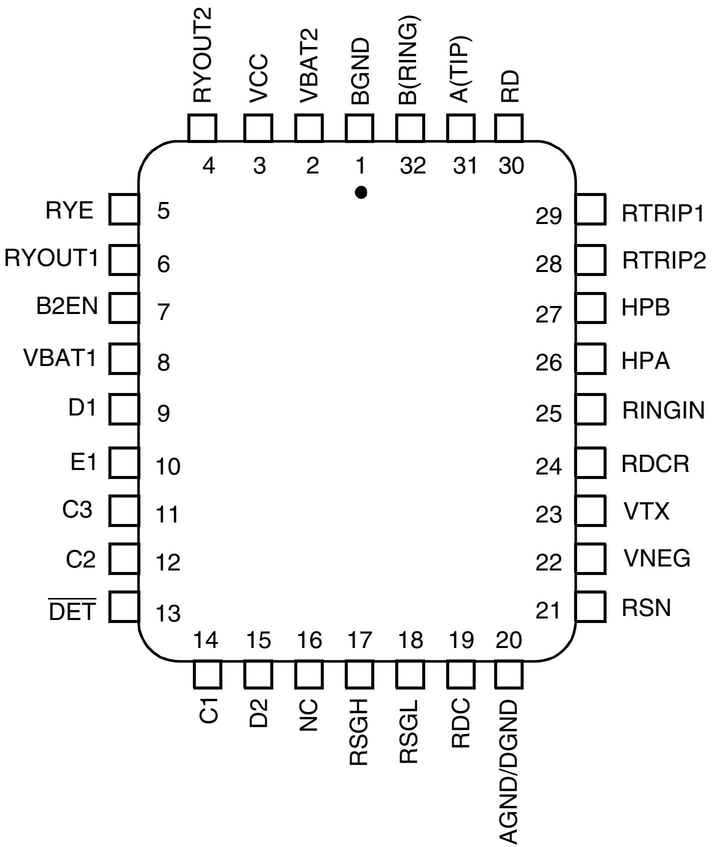
Note:

** Functionality of the device from 0°C to +70°C is guaranteed by production testing.*

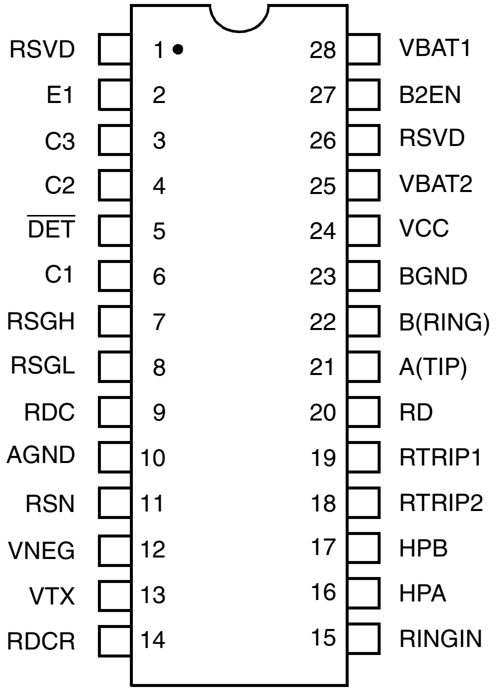
CONNECTION DIAGRAMS

Top View

32-Pin PLCC



28-Pin SOIC



Notes:

1. *Pin 1 is marked for orientation.*
2. *NC = No connect*
3. *RSVD = Reserved. Do not connect to this pin.*

PIN DESCRIPTIONS

Pin Names	Type	Description
AGND/DGND	Gnd	Analog and digital ground are connected internally to a single pin.
A(TIP)	Output	Output of A(TIP) power amplifier.
B2EN	Input	V_{BAT2} enable. Logic Low enables operation from V_{BAT2}. Logic High enables operation from V_{BAT1}. TTL compatible.
BGND	Gnd	Battery (power) ground
B(RING)	Output	Output of B(RING) power amplifier.
C3–C1	Input	Decoder. TTL compatible. C3 is MSB and C1 is LSB.
D1	Input	Relay1 control. TTL compatible. Logic Low activates the Relay1 relay driver.
D2	Input	(Option) Relay2 control. TTL compatible. Logic Low activates the Relay2 relay driver.
$\overline{DET}$	Output	Detector. Logic Low indicates that the selected detector is tripped. Logic inputs C3–C1 and E1 select the detector. Open-collector with a built-in 15 kΩ pull-up resistor.
E1	Input	(Option) A logic High selects the off-hook detector. A logic Low selects the ground-key detector. TTL compatible.
HPA	Capacitor	High-pass filter capacitor. A(TIP) side of high-pass filter capacitor.
HPB	Capacitor	High-pass filter capacitor. B(RING) side of high-pass filter capacitor.
RD	Resistor	Detect resistor. Threshold modification and filter point for the off-hook detector.
RDC	Resistor	DC feed resistor. Connection point for the DC-feed current programming network, which also connects to the receiver summing node (RSN). V_{RDC} is negative for normal polarity and positive for reverse polarity.
RDCR	—	Connection point for feedback during ringing.
RINGIN	Input	Ring Signal Input. Pin for ring signal input. Square-wave shaped by external RC filter. Requires 50% duty cycle. CMOS-compatible input.
RSGH	Input	Saturation Guard High. Pin for resistor to adjust Open Circuit voltage when operating from V_{BAT1}.
RSGL	Input	Saturation Guard Low. Pin for resistor to adjust the anti-saturation cut-in voltage when operating from both $V_{BAT1\text{ and }}V_{BAT2}$.
RSN	Input	The metallic current (AC and DC) between A(TIP) and B(RING) is equal to 1000 x the current into this pin. The networks that program receive gain, two-wire impedance, and feed resistance all connect to this node.
RTRIP1	Input	Ring-trip detector. Ring-trip detector threshold set and filter pin.
RTRIP2	Input	Ring-trip detector threshold offset (switch to V_{BAT1}). For power conservation in any nonringing state, this switch is open.
RYE	Output	Common Emitter of RYOUT1/RYOUT2. Emitter output of RYOUT1 and RYOUT2. Normally connected to relay ground.
RYOUT1	Output	Relay/switch driver. Open-collector driver with emitter internally connected to RYE.
RYOUT2	Output	(Option) Relay/switch driver. Open-collector driver with emitter internally connected to RYE.
VBAT1	Battery	Battery supply and connection to substrate.
VBAT2	Battery	Power supply to output amplifiers. Connect to off-hook battery through a diode.
VCC	Power	Positive analog power supply.
VNEG	Power	Negative analog power supply. This pin is the return for the internal VEE regulator.
VTX	Output	Transmit Audio. This output is a 0.5066 gain version of the A(TIP) and B(RING) metallic AC voltage. VTX also sources the two-wire input impedance programming network.

ABSOLUTE MAXIMUM RATINGS

Storage temperature	–55°C to +150°C
V_{CC} with respect to AGND/DGND	0.4 V to +7 V
V_{NEG} with respect to AGND/DGND	0.4 V to V_{BAT2}
V_{BAT2}	V_{BAT1} to GND
V_{BAT1} with respect to AGND/DGND:	
Continuous	+0.4 V to –80 V
10 ms	+0.4 V to –85 V
BGND with respect to AGND/DGND	+3 V to –3 V
A(TIP) or B(RING) to BGND:	
Continuous	V_{BAT1} –5 V to +1 V
10 ms (f = 0.1 Hz)	V_{BAT1} –10 V to +5 V
1 µs (f = 0.1 Hz)	V_{BAT1} –15 V to +8 V
250 ns (f = 0.1 Hz)	V_{BAT1} –20 V to +12 V
Current from A(TIP) or B(RING)	±150 mA
RYOUT1, RYOUT2 current	75 mA
RYOUT1, RYOUT2 voltage	RYE to +7 V
RYOUT1, RYOUT2 transient	RYE to +10 V
RYE voltage	BGND to V_{BAT1}
C3–C1, D2–D1, E1, B2EN, and RINGIN	
Input voltage	–0.4 V to V_{CC} + 0.4 V
Maximum power dissipation, continuous,	
T_A = 70°C, No heat sink (See note):	
In 32-pin PLCC package	1.67 W
In 28-pin SOIC package	1.25 W
Thermal Data:	θ_{JA}
In 32-pin PLCC package	45°C/W typ
In 28-pin SOIC package	60°C/W typ

Note: *Thermal limiting circuitry on chip will shut down the circuit at a junction temperature of about 165°C. The device should never see this temperature and operation above 145°C junction temperature may degrade device reliability. See the SLIC Packaging Considerations for more information.*

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices

Ambient temperature	0°C to +70°C*
V_{CC}	4.75 V to 5.25 V
V_{NEG}	–4.75 V to V_{BAT2}
V_{BAT1}	–40 V to –67 V
V_{BAT2}	–19 V to V_{BAT1}
AGND/DGND	0 V
BGND with respect to AGND/DGND	–100 mV to +100 mV
Load resistance on VTX to ground	20 kΩ min

The Operating Ranges define those limits between which the functionality of the device is guaranteed.

** Functionality of the device from 0°C to +70°C is guaranteed by production testing.*

ELECTRICAL CHARACTERISTICS

Description	Test Conditions (See Note 1)	Min	Typ	Max	Unit	Note
Transmission Performance						
2-wire return loss	200 Hz to 3.4 kHz (Test Circuit D)	26			dB	1, 4, 6
Z_{VTX}, analog output impedance			3	20	Ω	4
V_{VTX}, analog output offset voltage		–50		+50	mV	
Z_{RSN}, analog input impedance			1	20	Ω	4
Overload level, 2-wire and 4-wire, off hook	Active state	2.5			Vpk	2a
Overload level, 2-wire	On hook, R_{LAC} = 600 Ω	0.88			Vrms	2b
THD (Total Harmonic Distortion)	+3 dBm, BAT2 = –24 V		–64	–50	dB	5
THD, on hook, OHT state	0 dBm, R_{LAC} = 600 Ω, BAT1 = –67 V			–40		
Longitudinal Performance (See Test Circuit C)						
Longitudinal to metallic L-T, L-4 balance	200 Hz to 3.4 kHz	40			dB	
Longitudinal signal generation 4-L	200 Hz to 800 Hz, Normal polarity	40				
Longitudinal current per pin (A or B)	Active or OHT state	12	28		mArms	4
Longitudinal impedance at A or B	0 to 100 Hz, T_A = +25°C		25		Ω/pin	
Idle Channel Noise						
C-message weighted noise			+7	+14	dBrnC	
Psophometric weighted noise			–83	–76	dBmp	4
Insertion Loss and Four- to Four-Wire Balance Return Signal (See Test Circuits A and B)						
Gain accuracy 4- to 2-wire	0 dBm, 1 kHz	–0.20	0	+0.20	dB	3
Gain accuracy 2- to 4-wire and 4- to 4-wire	0 dBm, 1 kHz	–6.22	–6.02	–5.82		
Gain accuracy 4- to 2-wire	OHT state, on hook	–0.35	0	+0.35		
Gain accuracy 2- to 4-wire and 4- to 4-wire	OHT state, on hook	–6.37	–6.02	–5.77		
Gain accuracy over frequency	300 to 3400 Hz relative to 1 kHz	–0.10		+0.10		
Gain tracking	+3 dBm to –55 dBm relative to 0 dBm	–0.10		+0.10		3, 4
Gain tracking OHT state, on hook	0 dBm to –37 dBm +3 dBm to 0 dBm	–0.10 –0.35		+0.10 +0.35		3, 4 3
Group delay	0 dBm, 1 kHz		3		μs	1, 4, 6

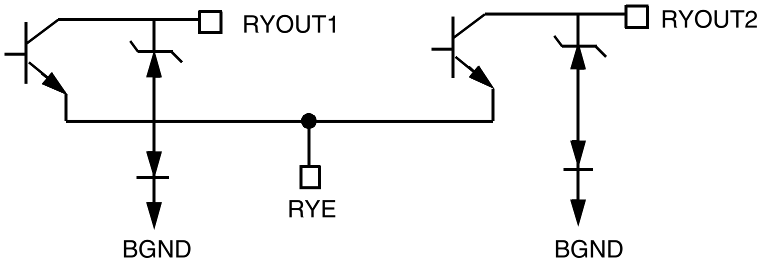
ELECTRICAL CHARACTERISTICS (CONTINUED)

Description	Test Conditions (See Note 1)	Min	Typ	Max	Unit	Note
Line Characteristics						
I_L, Loop-current accuracy	I_L in constant-current region, B2EN = 0	$0.9I_L$	I_L	$1.1I_L$	mA	
I_L, Long loops, Active state	R_{LDC} = 600 Ω, RSGL = open	20	21.7			
	R_{LDC} = 750 Ω, RSGL = short	20				
I_L, Accuracy, Standby state	$I_L = \dfrac{\lvert V_{BAT1}\rvert - 10\ \text{V}}{R_L + 400}$	$0.8I_L$	I_L	$1.2I_L$		
	I_L = constant-current region T_A = 25°C	18	27	39		
I_LLIM	Active, A and B to ground		55	110		
	OHT, A and B to ground		55			4
I_L, Loop current, Open Circuit state	R_L = 0			100	μA	
I_A, Pin A leakage, Tip Open state	R_L = 0			100		
I_B, Pin B current, Tip Open state	B to ground		34		mA	
V_A, Standby, ground-start signaling	A to –48 V = 7 kΩ, B to ground = 100 Ω	–7.5	–5		V	4
V_{AB}, Open Circuit voltage		42				7
Power Supply Rejection Ratio (V_{RIPPLE} = 100 mVrms), Active Normal State						
V_{CC}	50 Hz to 3400 Hz	33	50		dB	5
V_{NEG}	50 Hz to 3400 Hz	30	40			
V_{BAT1}	50 Hz to 3400 Hz	30	50			
V_{BAT2}	50 Hz to 3400 Hz	30	50			
Power Dissipation						
On hook, Open Circuit state	V_{BAT1}		48	100	mW	
On hook, Standby state	V_{BAT2}		55	80		9
On hook, OHT state	V_{BAT1}		200	300		
On hook, Active state	V_{BAT1}		220	350		
Off hook, Standby state	V_{BAT1} or V_{BAT2} R_L = 300 Ω		2000	2800		9
Off hook, OHT state	V_{BAT1} R_L = 300 Ω		2000	2200		
Off hook, Active state	V_{BAT2} R_L = 300 Ω		550	750		
Supply Currents						
I_{CC}, On-hook V_{CC} supply current	Open Circuit state		3.0	4.5	mA	
	Standby state		3.2	5.5		
	OHT state		6.2	8.0		
	Active state–normal		6.5	9.0		
I_{NEG}, On-hook V_{NEG} supply current	Open Circuit state		0.1	0.2		
	Standby state		0.1	0.2		
	OHT state		0.7	1.1		
	Active state–normal		0.7	1.1		
I_{BAT}, On-hook V_{BAT} supply current	Open Circuit state		0.45	1.0		
	Standby state		0.6	1.5		
	OHT state		2.0	4.0		
	Active state–normal		2.7	5.0		

ELECTRICAL CHARACTERISTICS (continued)

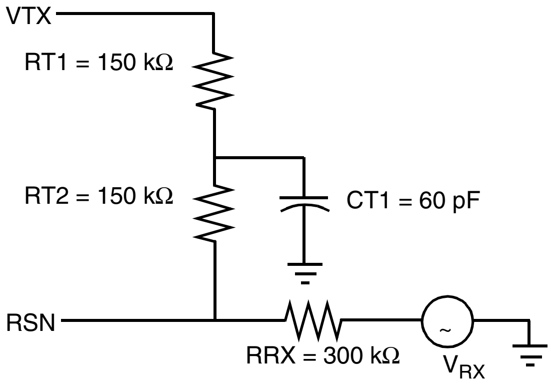
Description	Test Conditions (See Note 1)	Min	Typ	Max	Unit	Note
Logic Inputs (C3–C1, D2–D1, E1, and B2EN)						
V_{IH}, Input High voltage		2.0			V	
V_{IL}, Input Low voltage				0.8		
I_{IH}, Input High current		–75		40	µA	
I_{IL}, Input Low current		–400				
Logic Output $\overline{\text{DET}}$						
V_{OL}, Output Low voltage	I_{OUT} = 0.8 mA, 15 kΩ to V_{CC}			0.40	V	
V_{OH}, Output High voltage	I_{OUT} = –0.1 mA, 15 kΩ to V_{CC}	2.4				
Ring-Trip Detector Input						
Ring detect accuracy	$IRTD = \left(\frac{\lvert BAT1\rvert - 1}{RRT1} + 24\ \mu A\right) \bullet 335$	–10		+10	%	
Ring Signal						
V_{AB}, Ringing	Bat1 = –67 V, ringload = 1570 Ω	57	61		Vpk	
V_{AB} Ringing offset	V_{RINGIN} = 2.5 V		0		V	
$\Delta V_{AB}/\Delta V_{RINGIN}$ (RINGIN gain)			180		—	
Ground-Key Detector Thresholds						
Ground-key resistive threshold	B to ground	2	5	10	kΩ	
Ground-key current threshold	B to ground		11		mA	
Loop Detector						
R_{LTH}, Loop-resistance detect threshold	Active, V_{BAT1} Active, V_{BAT2} Standby	–20 –20 –12		20 20 12	%	8
Relay Driver Output (RELAY1 and 2)						
V_{OL}, On voltage (each output)	I_{OL} = 30 mA		+0.25	+0.4	V	
V_{OL}, On voltage (each output)	I_{OL} = 40 mA		+0.30	+0.8		4
I_{OH}, Off leakage (each output)	V_{OH} = +5 V			100	µA	
Zener breakover (each output)	I_Z = 100 µA	6.6	7.9		V	
Zener on voltage (each output)	I_Z = 30 mA		11			

RELAY DRIVER SCHEMATIC



Notes:

1. *Unless otherwise noted, test conditions are BAT1 = –67 V, BAT2 = –24 V, V_{CC} = +5 V, V_{NEG} = –5 V, R_L = 600 Ω, R_{DC1} = 80 kΩ, R_{DC2} = 20 kΩ, R_D = 75 kΩ, no fuse resistors, C_{HP} = 0.018 μF, C_{DC} = 1.2 μF, D_1 = D_2 = 1N400x, two-wire AC input impedance (ZSL) is a 600 Ω resistance synthesized by the programming network shown below. R_{SGL} = open, R_{SGH} = open, R_{DCR} = 2 kΩ, R_{RT1} = 430 kΩ, R_{RT2} = 12 kΩ, C_{RT} = 1.5 μF, R_{SLEW} = 150 kΩ, C_{SLEW} = 0.33 μF.*



2. *a. Overload level is defined when THD = 1%.*
   b. Overload level is defined when THD = 1.5%.
3. *Balance return signal is the signal generated at V_{TX} by V_{RX}. This specification assumes that the two-wire AC load impedance matches the programmed impedance.*
4. *Not tested in production. This parameter is guaranteed by characterization or correlation to other tests.*
5. *This parameter is tested at 1 kHz in production. Performance at other frequencies is guaranteed by characterization.*
6. *Group delay can be greatly reduced by using a Z_T network such as that shown in Note 1 above. The network reduces the group delay to less than 2 μs and increases 2WRL. The effect of group delay on linecard performance may also be compensated for by synthesizing complex impedance with the QSLAC or DSLAC device.*
7. *Open Circuit V_{AB} can be modified using RSGH.*
8. *R_D must be greater than 56 kΩ. Refer to Table 2 for typical value of R_{LTH}.*
9. *Lower power is achieved by switching into low-battery state in standby. Standby loop current is returned to V_{BAT1} regardless of the battery selected.*

Table 1. SLIC Decoding

State	C3 C2 C1	2-Wire Status	$(\overline{\text{DET}})$ Output E1 = 1	$(\overline{\text{DET}})$ Output E1 = 0	Battery Selection
0	0 0 0	Open Circuit	Ring trip	Ring trip	B2EN
1	0 0 1	Ringing	Ring trip	Ring trip	
2	0 1 0	Active	Loop detector	Ground key	
3	0 1 1	On-hook TX (OHT)	Loop detector	Ground key	
4	1 0 0	Tip Open	Loop detector	Ground key	B2EN = 1**
5	1 0 1	Standby	Loop detector	Ground key	V_{BAT1}
6*	1 1 0	Active Polarity Reversal	Loop detector	Ground key	B2EN
7*	1 1 1	OHT Polarity Reversal	Loop detector	Ground key	

Notes:

** Only –1 performance grade devices support polarity reversal.*

*** For correct ground-start operation using Tip Open, V_{BAT1} on-hook battery must be used.*

Table 2. User-Programmable Components

$Z_T = 500(Z_{2WIN} - 2R_F)$	Z_T is connected between the VTX and RSN pins. The fuse resistors are R_F, and Z_{2WIN} is the desired 2-wire AC input impedance. When computing Z_T, the internal current amplifier pole and any external stray capacitance between VTX and RSN must be taken into account.
$Z_{RX} = \frac{Z_L}{G_{42L}} \bullet \frac{1000 \bullet Z_T}{Z_T + 500(Z_L + 2R_F)}$	Z_{RX} is connected from V_{RX} to R_{SN}. Z_T is defined above, and G_{42L} is the desired receive gain.
$R_{DC1} + R_{DC2} = \frac{2500}{I_{LOOP}}$	R_{DC1}, R_{DC2}, and C_{DC} form the network connected to the RDC pin. I_{LOOP} is the desired loop current in the constant-current region.
$R_{DCR1} + R_{DCR2} = \frac{3000}{Iringlim}$ $C_{DC} = 19\ ms \bullet \frac{R_{DC1} + R_{DC2}}{R_{DC1}R_{DC2}}$	R_{DCR1}, R_{DCR2}, and C_{DCR} form the network connected to the RDCR pin. See Applications Circuit for these components.
$C_{DCR} = \frac{R_{DCR1} + R_{DCR2}}{R_{DCR1}R_{DCR2}} \bullet 150\ \mu s$	C_{DCR} sets the ringing time constant, which can be between 15 µs and 150 µs.
$R_D = R_{LTH} \bullet 12.67$ for high battery state	R_D is the resistor connected from the RD pin to GND and R_{LTH} is the loop-resistance threshold between on-hook and off-hook detection. R_D should be greater than 56 kΩ to guarantee detection will occur in the Standby state. Choose the value of R_D for high battery state; then use the equation for R_{LTH} to find where the threshold is for low battery.
Loop-Threshold Detect Equations	
$R_{LTH} = \frac{R_D}{12.67}$ for high battery	This is the same equation as for R_D in the preceding equation, except solved for R_{LTH}.
$R_{LTH} = \frac{R_D}{11.37}$ for low battery	For low battery, the detect threshold is slightly higher, which will avoid oscillating between states.
$R_{LTH} = \frac{\lvert V_{BAT1} \rvert - 10}{915} \bullet R_D - 400 - 2R_F$	R_{LTH} standby < R_{LTH} active V_{BAT1} < R_{LTH} active V_{BAT2}, which will guarantee no unstable states under all operating conditions. This equation will show at what resistance the standby threshold will be; it is actually a current threshold rather than a resistance threshold, which is shown by the Vbat dependency.

DC FEED CHARACTERISTICS

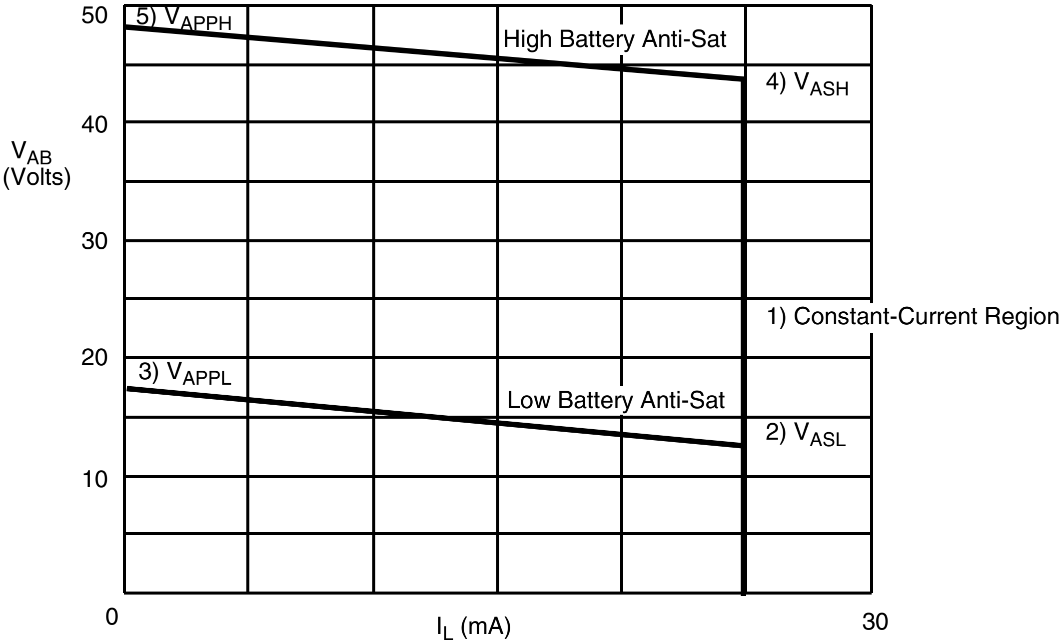


Figure 1. Typical V_{AB} vs. I_L DC Feed Characteristics

$$R_{DC} = R_{DC1} + R_{DC2} = 20\ \text{k}\Omega + 80\ \text{k}\Omega = 100\ \text{k}\Omega$$

$$(V_{BAT1} = -67\ \text{V},\ V_{BAT2} = -24\ \text{V})$$

Notes:

1. *Constant-current region:* $V_{AB} = I_L R_L = \frac{2500}{RDC} R_L$; *where* $R_L = R_L + 2R_F$

2. *Low battery* $V_{ASL} = \frac{1000 \bullet (104 \bullet 10^3 + R_{SGL})}{6720 \bullet 10^3 + (80 \bullet R_{SGL})}$; *where R_{SGL} = resistor to GND, B2EN = logic Low.*

   Anti-sat region: $V_{ASL} = \frac{1000 \bullet (R_{SGL} - 56 \bullet 10^3)}{6720 \bullet 10^3 + (80 \bullet R_{SGL})}$; *where R_{SGL} = resistor to V_{CC}, B2EN = logic Low.*

   R_{SGL} to V_{CC} must be greater than 100 kΩ.

3. $V_{APPL} = 4.17 + V_{ASL}$

   $$I_{LOOPL} = \frac{V_{APPL}}{\frac{(R_{DC1} + R_{DC2})}{600} + 2R_F + R_{LOOP}}$$

4. *High battery* $V_{ASH} = V_{ASHH} + V_{ASL}$

   Anti-sat region: $V_{ASHH} = \frac{1000 \bullet (70 \bullet 10^3 + R_{SGH})}{1934 \bullet 10^3 + (31.75 \bullet R_{SGH})}$; *where R_{SGH} = resistor to GND, B2EN = logic High.*

   $V_{ASHH} = \frac{1000 \bullet (R_{SGH} + 2.75 \bullet 10^3)}{1934 \bullet 10^3 + (31.75 \bullet R_{SGH})}$; *where R_{SGH} = resistor to V_{CC}, B2EN = logic High.*

   R_{SGH} to V_{CC} must be greater than 100 kΩ.

5. $V_{APPH} = 4.17 + V_{ASH}$

   $$I_{LOOPH} = \frac{V_{APPH}}{\frac{(R_{DC1} + R_{DC2})}{600} + 2R_F + R_{LOOP}}$$

RING-TRIP COMPONENTS

$R_{RT2} = 12\ \text{k}\Omega$

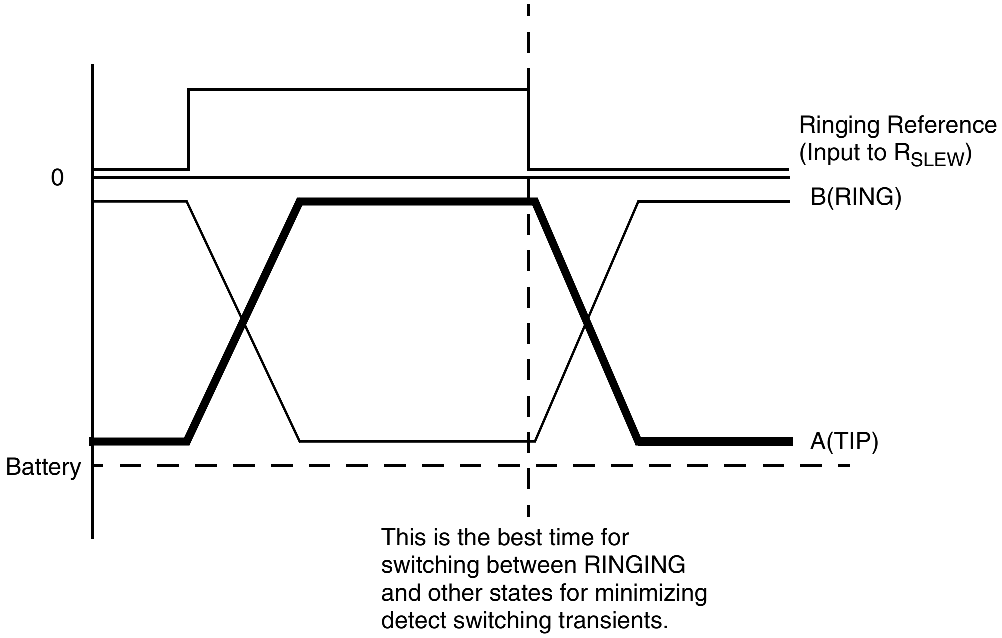
$C_{RT} = 1.5\ \mu\text{F}$

$$R_{RT1} = 320 \bullet CF \bullet \frac{V_{BAT1}}{Vbat - 5 - (24\ \mu A \bullet 320 \bullet CF \bullet (R_{LRT} + 150 + 2R_F))} \bullet (R_{LRT} + 150 + 2R_F)$$

where R_{LRT} = Loop-detection threshold resistance for ring trip and CF = Crest factor of ringing signal (≈ 1.25)

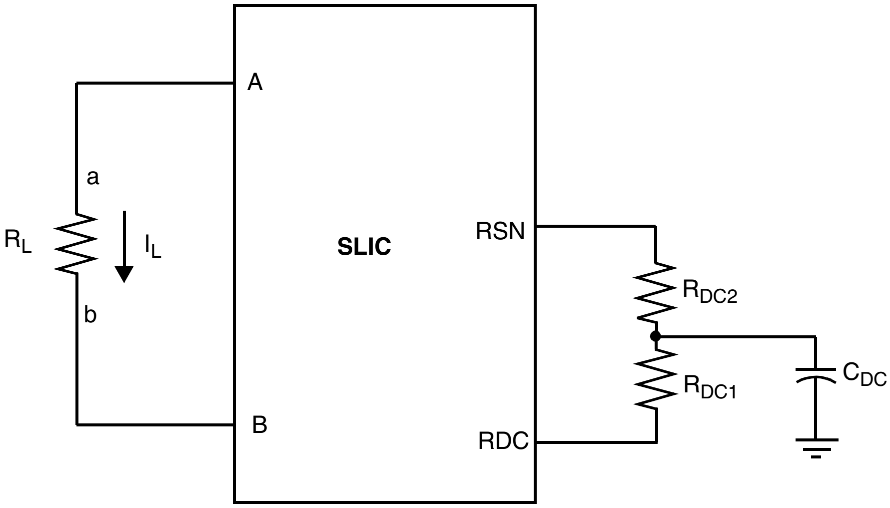
R_{SLEW}, C_{SLEW}

Ring waveform rise time ≈ 0.214 • (R_{SLEW} • C_{SLEW}) ≈ tr.
For a 1.25 crest factor @ 20 Hz, tr ≈ 10 mS.
∴ (R_{SLEW} = 150 kΩ, C_{SLEW} = 0.33 μF.)
C_{SLEW} should be changed if a different crest factor is desired.



This is the best time for switching between RINGING and other states for minimizing detect switching transients.

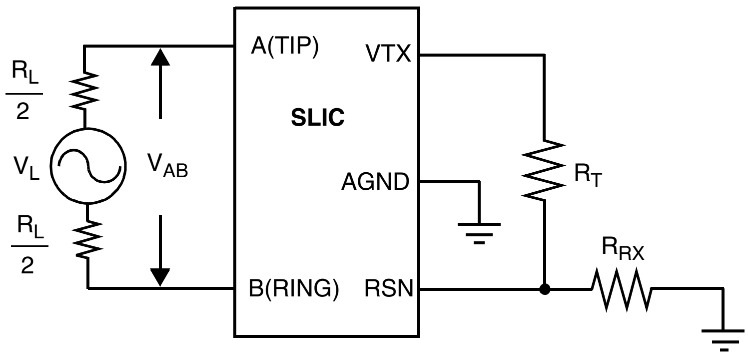
Figure 2. Ringing Waveforms



Feed current programmed by R_{DC1} and R_{DC2}

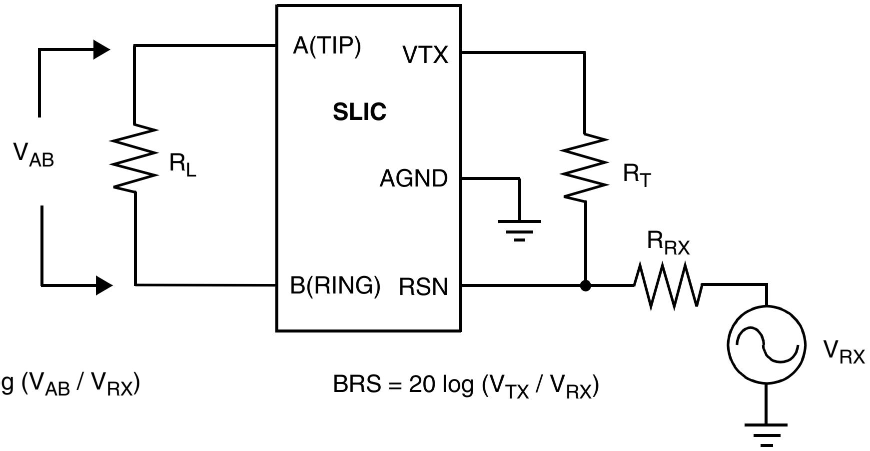
Figure 3. Feed Programming

TEST CIRCUITS



$I_{L2-4} = 20 \log (V_{TX} / V_{AB})$

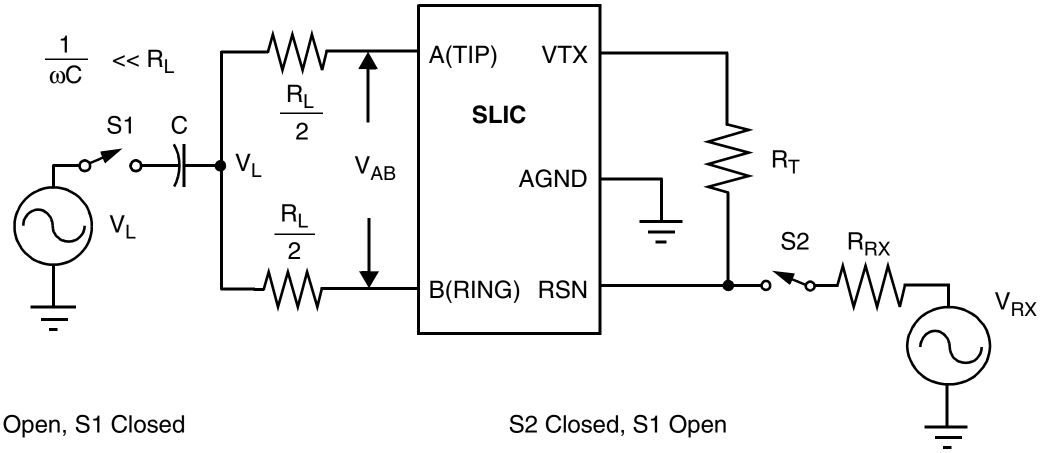
A. Two- to Four-Wire Insertion Loss



$I_{L4-2} = 20 \log (V_{AB} / V_{RX})$

$BRS = 20 \log (V_{TX} / V_{RX})$

B. Four- to Two-Wire Insertion Loss and Four- to Four-Wire Balance Return Signal



S2 Open, S1 Closed

L-T Long. Bal. = $20 \log (V_{AB} / V_L)$

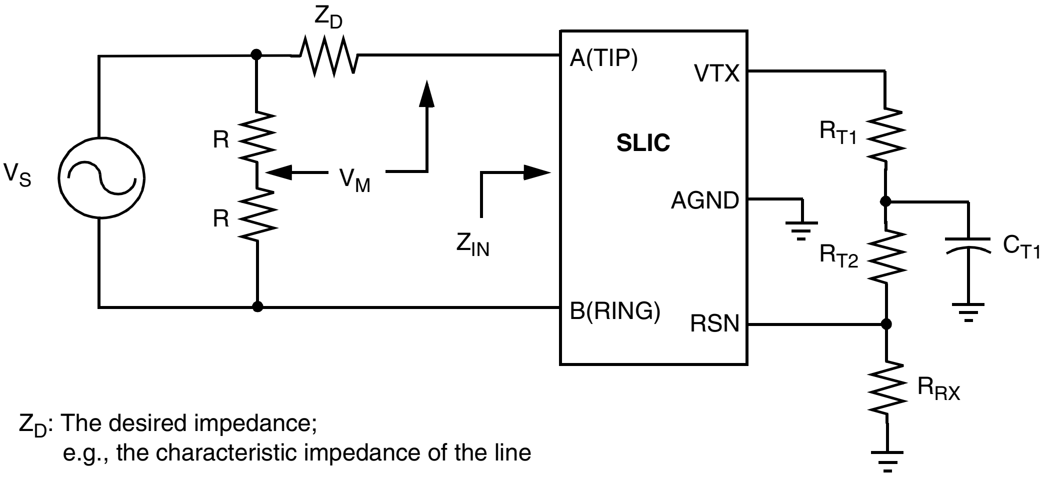
L-4 Long. Bal. = $20 \log (V_{TX} / V_L)$

S2 Closed, S1 Open

4-L Long. Sig. Gen. = $20 \log (V_L / V_{RX})$

C. Longitudinal Balance

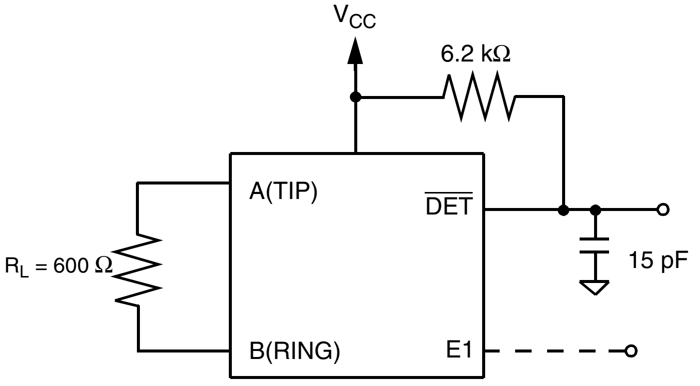
TEST CIRCUITS (continued)

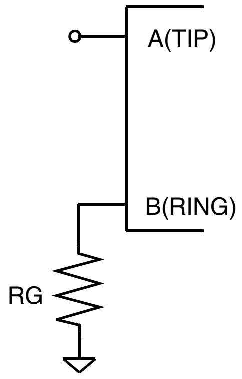


Z_D: The desired impedance;
e.g., the characteristic impedance of the line

Return loss = –20 log (2 V_M / V_S)

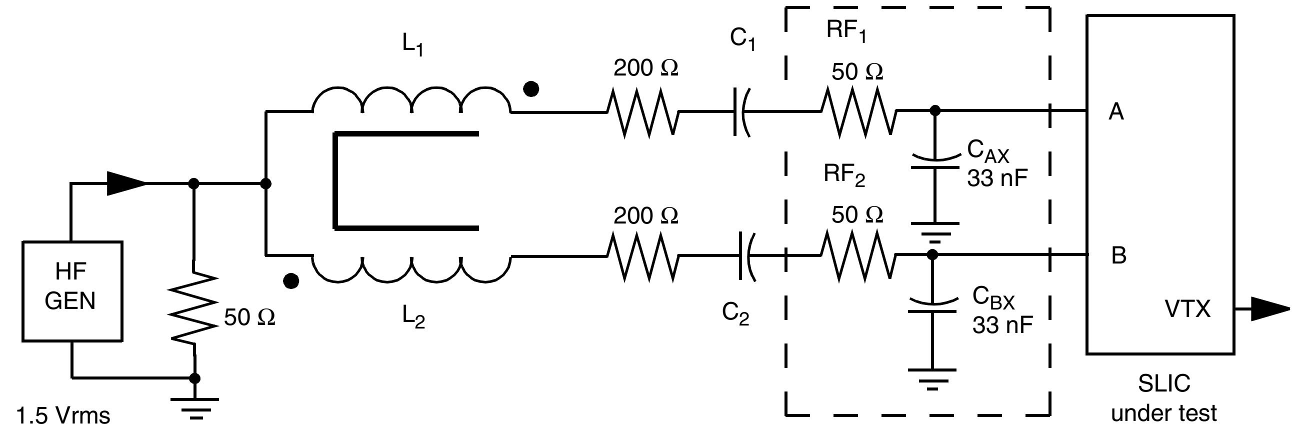
D. Two-Wire Return Loss Test Circuit





E. Loop-Detector Switching

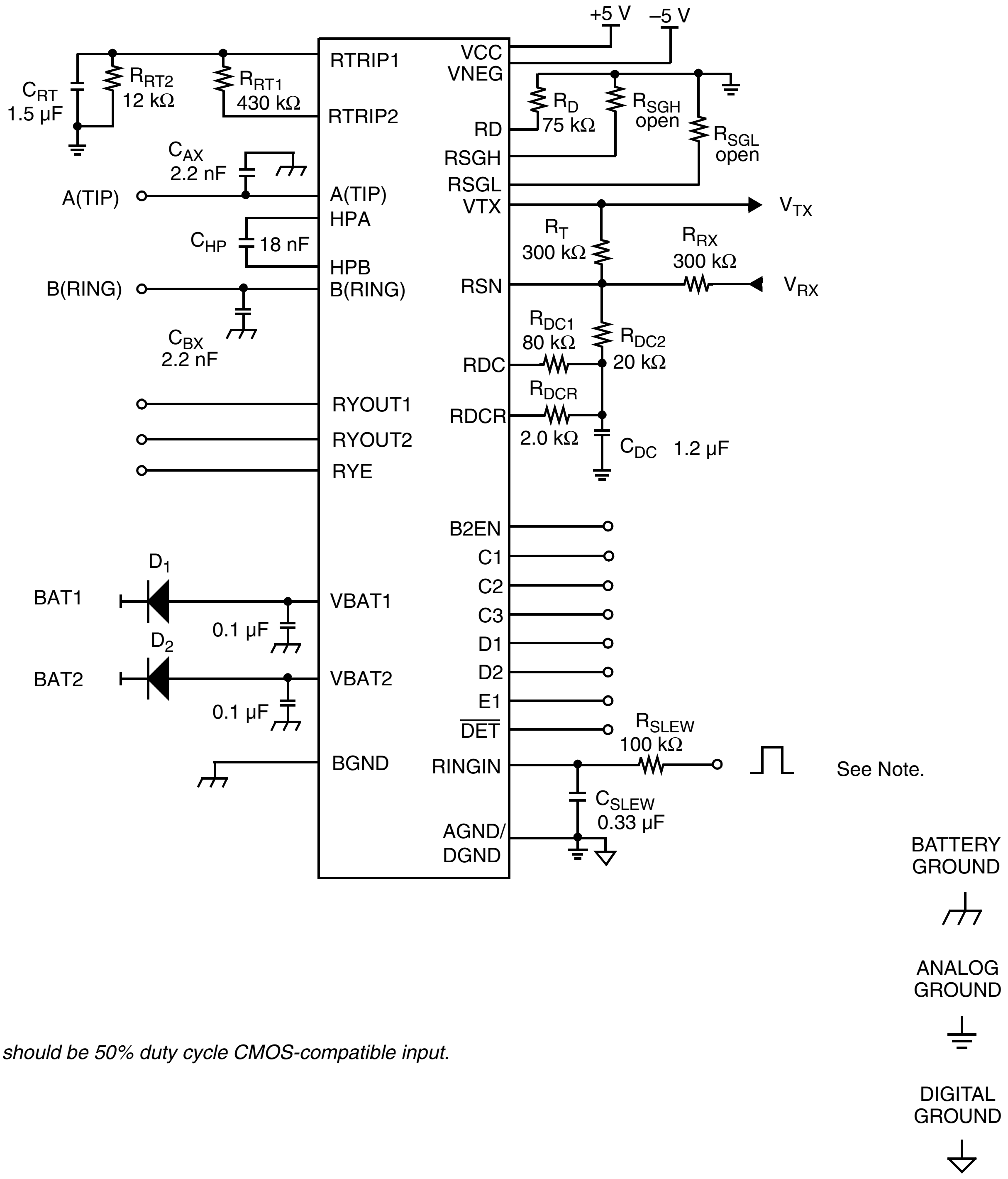
F. Ground-Key Switching



1.5 Vrms
80% Amplitude
Modulated
100 kHz to 30 MHz

G. RFI Test Circuit

TEST CIRCUITS (continued)

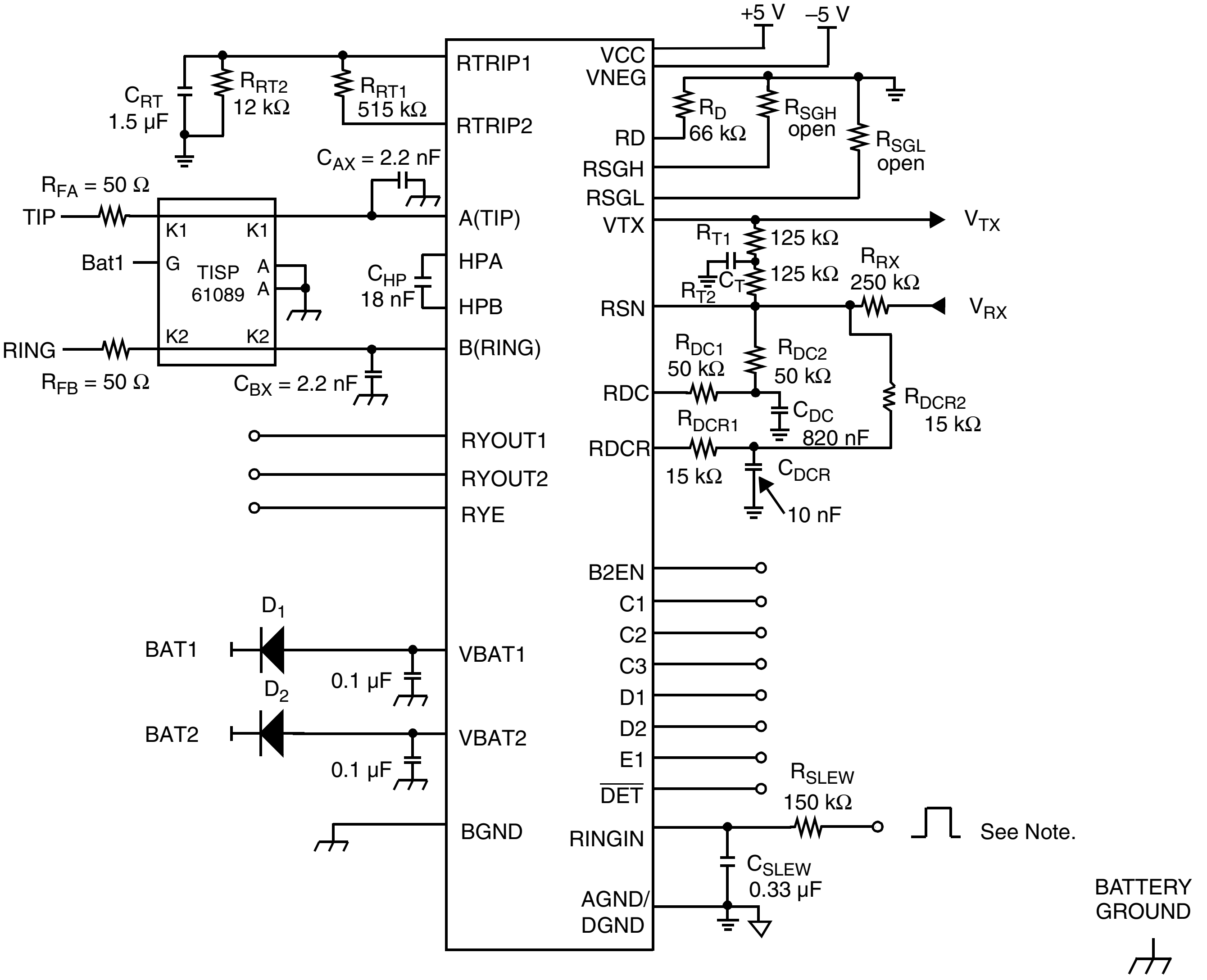


Note:

The input should be 50% duty cycle CMOS-compatible input.

H. Am79R70 Test Circuit

APPLICATION CIRCUIT



Assumptions:

1. 1.25 CF
2. 25 mA I_{LOOP}
3. 100 mA Ringing Current Limit
4. 5.2 kΩ High Battery Loop Threshold
5. 925 Ω Ringing Loop Threshold
6. 600 Ω Two-wire Impedance, 600 Ω Z_L
7. $G_{42L} = 1$
8. –67 V Vbat1, –24 V Vbat2

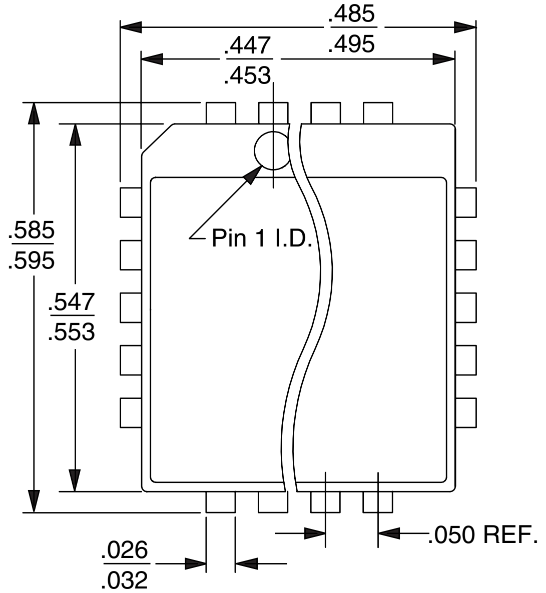
Note:

The input should be 50% duty cycle CMOS-compatible input.

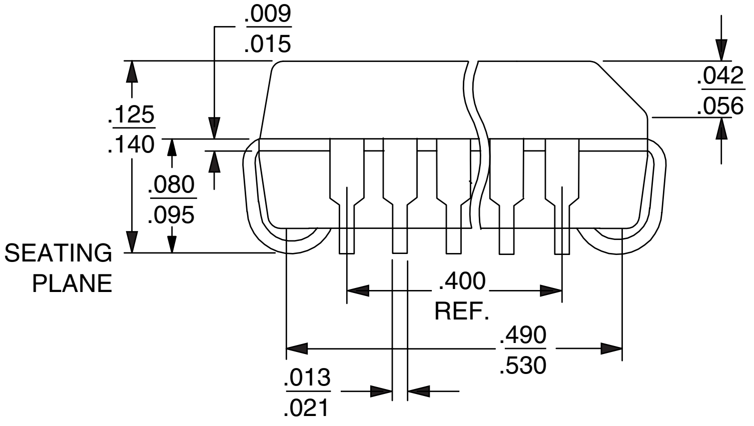
I. Application Circuit

PHYSICAL DIMENSIONS

PL032



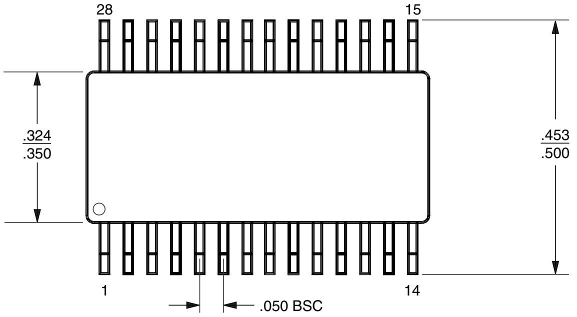
TOP VIEW

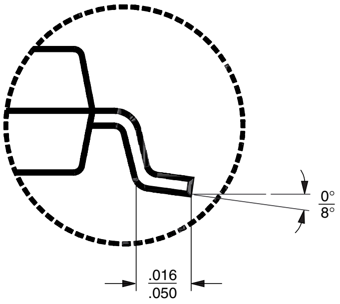


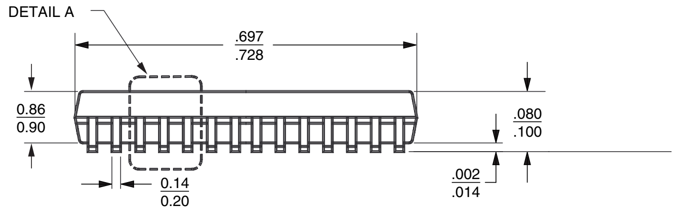
SIDE VIEW

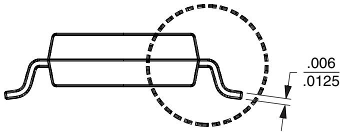
16-038FPO-5
PL 032
DA79
6-28-94 ae

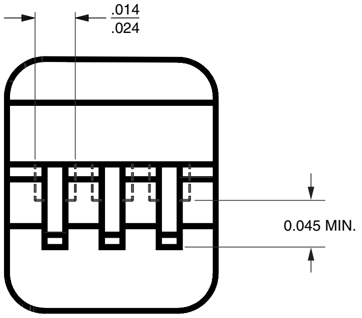
SOW28











DETAIL A

16-038-SO28-2_AC
SOW28
DF87
9-3-97 lv

REVISION SUMMARY

Revision A to Revision B

- Minor changes were made to the data sheet style and format to conform to AMD standards.

Revision B to Revision C

- The 28-pin SOIC information and package was added to the Ordering Information and the Connection Diagrams sections.
- The physical dimensions (PL032 and SOW28) were added to the Physical Dimensions section.
- Updated the Pin Description table to correct inconsistencies.

Revision C to Revision D

- Changed Ring-Trip Components equation from:

$$R_{RT1} = 300 \bullet CF \bullet \frac{V_{BAT1}}{Vbat - 3.5 - (15\ \mu A \bullet 300 \bullet CF \bullet (R_{LRT} + 150 + 2R_F))} \bullet (R_{LRT} + 150 + 2R_F)$$

To:

$$R_{RT1} = 320 \bullet CF \bullet \frac{V_{BAT1}}{Vbat - 5 - (24\ \mu A \bullet 320 \bullet CF \bullet (R_{LRT} + 150 + 2R_F))} \bullet (R_{LRT} + 150 + 2R_F)$$

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